REMARKS

The specification has been rewritten to supply the new title required.

With regard to the Examiner's statement that the reference named on page 2, line 12, of the specification has not been considered since it was not included in an Information Disclosure Statement (IDS), that reference actually was considered. However, the number given in the specification was the patent number, not the publication number which was listed in an Information Disclosure Statement (IDS) already filed and considered, and that has been corrected in this amendment.

Claims 1-3 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirano et al., U.S. Publication No. 2002/0153618, in view of Hsuan et al., U.S. Patent No. 6,323,546. Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over Hirano et al., in view of Hsuan et al., and Akram et al., U.S. Patent No. 6,493,229. Claim 5 was rejected under 35 U.S.C. § 103 (a) as being unpatentable over Hirano et al. in view of Hsuan et al. and Ohuchi et al., U.S. Patent No. 5,999,413.

Claim 1 provides that the insulator resin film contacts side portions of each of the protruding electrodes and that the conductive film contacts the top portion of the protruding electrodes.

In contrast, Hirano et al. discloses that the insulator resin film 11 in Fig. 3 does **not** even contact the protruding electrodes 12. Furthermore, there is **no** conductive film contacting the top portion of the protruding electrodes 12.

In addition, Hirano et al. teaches a technique for improving a CSP (Chip Size Package) type semiconductor device having a face-up structure. The semiconductor chip 7A is mounted on the side of a chip mounting surface 1A of the substrate 1 by an adhesive 9 on the rear surface of the semiconductor chip with the circuit forming surface 7A1 up, (pages 3-4, paragraph [0056]).

The mounting method of the present invention, as described in the application, is opposite to Hirano et al.:

"a semiconductor chip 15 having a plurality of film electrodes 15a on the rear surface of the semiconductor chip 15 and a plurality of bump front electrodes 15b protruding from the front surface of the semiconductor chip 15;...", (page 6, lines 20-23 in the present specification).

In contrast, Hirano et al. teaches that the substrate 1 has bump electrodes and the semiconductor chip 7A does not have bump electrodes.

According to the present specification, the invention includes:

"an insulator resin film 16 formed on entire surfaces of the semiconductor chip 15 while exposing the film electrodes 15a and the top surfaces of the bump front electrodes 15b; and a conductive resin film 17 formed on the front side of the semiconductor chip 15, or on the top surfaces of the bump front electrodes 15b. The conductive resin film 17 is configured as a plurality of interconnect lines connected to the bump front electrodes 15b", (page 6, line 23 to page 7, line 6).

Hirano et al. does not teach the use of film electrodes in Fig. 3. In Hirano et al., the bump electrodes 12 are exposed from the substrate 1.

According to the present invention, the bump front electrode 15b is exposed from the insulator resin film 16.

Hirano et al. does not teach any film on top of the bump electrodes 12. However, the structure of the present invention includes the conductive resin film 17.

Hsuan et al. teaches the structure and method of forming bumps 60 on the rear side of the substrate 36 as shown in Fig. 2H.

According to claim 1 of the present invention, the film electrodes 15a are disposed on the rear surface of the semiconductor chip 15.

Hirano et al. teaches that the rear side of the semiconductor chip 7A is bonded onto the substrate 1 as shown in Fig. 3. However, the substrate 1 is an interconnection substrate or generally known as an "interposer", which is used for interconnection between the lands on a printed circuit board and chip electrodes.

According to claim 2 of the present invention, the semiconductor chip is mounted on a printed circuit board, with the rear surface opposing the printed circuit board.

In connection with claim 3, Hirano et al. teaches that the bonding wire 10 is used to connect the bonding pad 8 of the semiconductor chip 7A and the wire-connecting pad 3 of the substrate 1.

The interconnection 2 connects the wire connecting pad 3 and the bump connecting land 4. The bump electrode 12 is disposed under the bump connecting land 4 through the connecting hole 5.

The wire 10 is therefore used within a semiconductor package, and does not connect the bonding pad 8 of the semiconductor chip 7A and a land of a printed circuit board.

In connection with claim 4, Hirano et al. teaches the bump electrode 12 in Fig. 3, which is disposed on the substrate 1.

According to the present invention, protruding electrodes are disposed on the semiconductor chip, as defined in claim 1 and in claim 4, depending from claim 1.

Akram et al. teaches a structure interposing the ball array 624 and the solder ring heat sink 628 between the printer circuit boards (PCBs). However, the integrated circuit chip 312 is simply mounted on one PCB, leaving a space between the chip and another PCB.

However, according to claim 4 of the present invention, the semiconductor chip is sandwiched between and contacts a pair of printed circuit boards.

Ohuchi et al. teaches that the structure having a side surface of the semiconductor chip 21 is covered with a sealing resin layer 26.

Hirano et al. teaches that the structure having a side surface of the semiconductor chip 7A is covered with a resin sealing body 11.

However, according to claim 5 of the present invention, a portion of a side surface of the semiconductor chip is exposed from the insulator resin film.

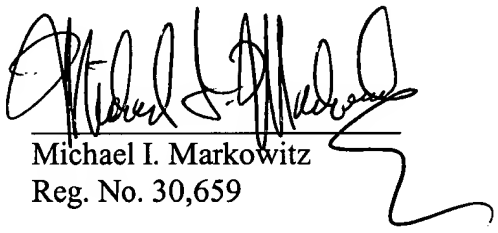
CLOSING

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that independent claim 1 is in condition for allowance, as well as those claims dependent therefrom. Passage of this case to allowance is earnestly solicited.

However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper, not fully covered by an enclosed check, may be charged on Deposit Account 50-1290.

Respectfully submitted,



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